

ABSTRACT

Sub A2 A digital television/local bus interface logic supports handling of progressive scan digital television (DTV) data with non-tearing. The interface logic provides a dual frame buffer DTV architecture in which a pair of DTV/local bus frame buffers alternate functions: one frame buffer stores incoming progressive scan DTV data and the other frame buffer stores the outgoing progressive scan DTV data. Incoming DTV data is written to one frame buffer. When a refresh of a display device reaches a programmed position of the display device, the interface logic determines which frame buffer is being updated by the incoming DTV data. The outgoing DTV data is then read from an opposite frame buffer and transmitted to the display device. The dual frame buffer DTV architecture insures that the outgoing DTV data to be delivered to the display device includes a whole frame so as to prevent tearing. Outgoing DTV data is synchronized to a refresh rate of a graphics controller coupled to the interface logic. The interface logic receives a horizontal sync signal and a vertical sync signal from the graphics controller for monitoring refresh of the display device. The interface logic in effect decouples the refresh rate of the incoming DTV data from the refresh rate of the graphics controller. Non-tearing may therefore be accomplished while optimizing the refresh rate of the outgoing DTV data. The interface logic also provides an architecture for transferring decoded DTV data over a local bus to the graphics controller. The interface logic thus eliminates the need for a video port cable between a graphics controller and a television tuner and the need for a non-standard graphics controller video port. Further, the interface logic may be configured to accommodate multiple DTV data streams, permitting scalable picture-in-picture (PIP) functionality.